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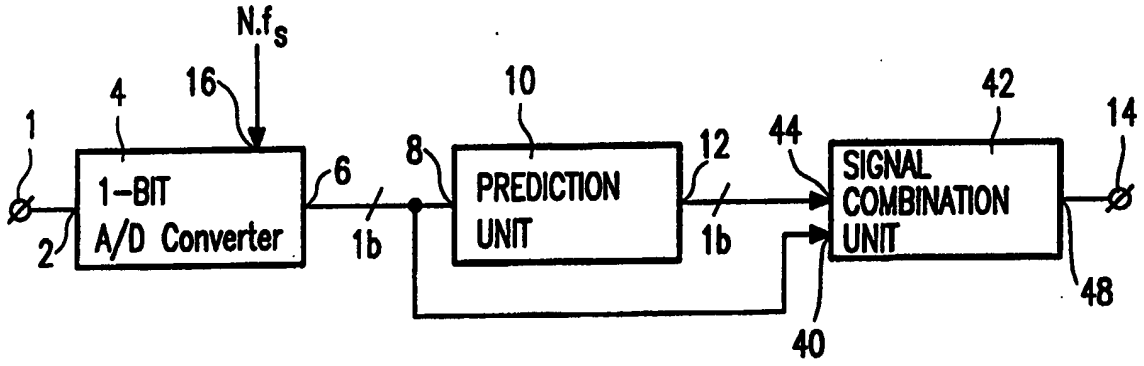

(57) Abstract

A data processing apparatus is disclosed for data processing an audio signal. The data processing apparatus comprises an input terminal (1) for receiving the audio signal, a 1-bit A/D converter (4) for A/D converting the audio signal so as to obtain a bitstream signal, a prediction unit (10) for carrying out a prediction step on the bitstream signal so as to obtain a predicted bitstream signal, a signal combination unit (42) for combining the bitstream signal and the predicted bitstream signal so as to obtain a residue bitstream signal, and an output terminal (14) for supplying the residual bitstream signal (Figure 1). Further, a recording apparatus (Figure 4) and a transmitter apparatus (Figure 5) comprising the data processing apparatus are disclosed. Other data processing apparatuses can be found in the figures 18, 19 and 20. In addition, another data processing apparatus (Figure 7) for converting the residue bitstream signal into an audio signal is disclosed, as well as a reproducing apparatus (Figure 9) and a receiver apparatus (Figure 10) comprising the other data processing apparatus.

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Data processing of a bitstream signal

The invention relates to a data processing apparatus for data processing an audio signal, to a data processing method, a transmitter comprising the data processing apparatus, a transmitter in the form of a recording apparatus, a record carrier, to second data processing apparatus for reconverting an input signal into a replica of the audio signal, to a receiver comprising the second data processing apparatus, to a receiver in the form of a reproducing apparatus and to a transmission signal comprising a data compressed residual bitstream signal.

Data processing an audio signal is well known in the art. Reference is made in this respect to EP-A 402,973, document D1 in the list of related documents. The document describes a subband coder, in which an audio signal is A/D converted with a specific sampling frequency, such as 44.1 kHz, and the resulting samples in de form of eg. 24 bits wide words of the audio signal, are supplied to a subband splitter filter. The subband splitter filter splits the wideband digital audio signal into a plurality of relatively narrow band subband signals. Using a psycho acoustic model, a masked threshold is derived and blocks of samples of the subband signals are subsequently quantised with a specific number of bits per sample for each block of the subband signals, in response to said masked threshold, resulting in a significant data compression of the audio signal to be transmitted. The data compression carried out is based on 'throwing away' those components in the audio signal that are inaudible and is thus a lossy compression method. The data compression described in document D1 is a rather intelligent data compression method and requires a substantial number of gates or instructions, when realized in hard or software respectively, so that it is expensive. Moreover, the subsequent expansion apparatus also requires a substantial number of gates or instructions, when realized in hardware or software respectively.

The invention aims at providing a data processing apparatus for processing an audio signal such that it can be data compressed by a lossless coder in a

relatively simple way. Further, the invention aims at providing a corresponding data processing apparatus for reconverting the processed bitstream signal into a replica of the audio signal.

The data processing apparatus in accordance with the invention comprises

- input means for receiving the audio signal,
- conversion means for carrying out a conversion on the audio signal so as to obtain a 1-bit bitstream signal, the conversion means comprising sigma-delta modulator means,
- prediction means for carrying out a prediction step on a signal so as to obtain a predicted bitstream signal,
- signal combination means for combining the bitstream signal and the predicted bitstream signal so as to obtain a residual bitstream signal, and
- output means for supplying the residual bitstream signal.

The invention is based on the following recognition. Bitstream signals take up a considerable amount of capacity. To illustrate this: in a current proposal for a new standard for an optical audio disk, the disk will contain two channels of bitstream converted audio signals, sampled at $64.f_s$, where $f_s = 44.1$ kHz. This corresponds to a rate four times higher than a current CD audio disk. As discussed in an earlier filed but not yet published patent application no. 96202807.2 in the name of applicant, document D7 in the list of related documents that can be found at the end of this description, already low complexity lossless coding algorithms, such as fixed Huffman table coding, are able to reduce this capacity to a certain extent. Experiments have revealed that even higher lossless compression ratios can be obtained using more sophisticated, more complex algorithms, such as Lempel-Ziv.

Mainly in audio/speech coding, linear prediction is known to be a powerful technique. By removing redundancy from a speech/audio signal prior to quantization, the entropy of signal after quantization can be significantly reduced. The signals at the input and output of a predictor are either in a floating point or a multi bit representation.

In lossless coding of bitstream signals, the complexity of the algorithm, especially at the decoder side is of importance. However, generally, the performance of the lossless coding algorithm is closely related to its complexity.

In accordance with the invention, prediction is used on bitstream signals. ie. signals with only two different representation symbols, either '0' or '1'. This has the

advantage of an increase of lossless compression performance, for only a marginal extra complexity.

Experiments have revealed that already a third order prediction has considerable effect on the statistics of the resulting signal. By means of prediction, as a preprocessing step, prior to data compression, the probability of a '1'-bit can be brought down from 50 % to about 20 %. The effect of this is that the output of the apparatus in accordance with the invention contains long runs of 'zeroes', which can be exploited by simple Huffman coding or run-length coding.

The audio signal can be applied in analog form or in digital form. When A/D converting, in accordance with the invention, an analog audio signal with a 1-bit A/D converter (also named: bitstream converter or sigma-delta modulator), the audio signal to be A/D converted is sampled with a frequency which is generally a multiplicity of the frequency of 44.1 kHz or 48 kHz. The output signal of the 1-bit A/D converter is a binary signal, named bitstream signal. When the audio signal is supplied in digital form, sampled at eg. 44.1 kHz, the samples being expressed in eg. 16 bits per sample, this digital audio signal is oversampled with a frequency which is again a multiplicity of this sampling frequency of 44.1 kHz (or 48 kHz), which results in the 1-bit bitstream signal.

Converting an audio signal into a 1-bit bitstream signal has a number of advantages. Bitstream conversion is a high quality encoding method, with the possibility of a high quality decoding or a low quality decoding with the further advantage of a simpler decoding circuit. Reference is made in this respect to the publications 'A digital decimating filter for analog-to-digital conversion of hi-fi audio signals', by J.J. van der Kam, document D2 in the list of related documents, and 'A higher order topology for interpolative modulators for oversampling A/D converters', by Kirk C.H. Chao et al, document D3 in the list of related documents.

1-bit D/A converters are used in CD players, as an example, to reconvert the bitstream audio signal into an analog audio signal. The audio signal recorded on a CD disk is however not data compressed, prior to recording on the disk.

It is well known in the art that the resulting bitstream signal of the 1-bit A/D converter is, roughly said, a random signal which has a 'noisy-like' frequency spectrum. Such types of signals are hard to data compress.

Surprisingly, however, it was established that applying a prediction step, prior to data compression, eg. using a lossless coder, a significant data reduction could be obtained, in spite of the noisy character of the bitstream signal from the 1-bit A/D converter.

These and other aspects of the invention will be apparent from and elucidated further with reference to the embodiments described in the following figure description, in which

figure 1 shows an embodiment of the data processing apparatus,

figure 2 shows part of an embodiment of a prediction unit for use in the apparatus of figure 1,

figure 3 shows an embodiment of the prediction unit and the signal combination unit incorporated in the data processing apparatus,

figure 4 shows the data processing apparatus of figure 1 incorporated in a recording apparatus for recording the residual bitstream signal on a record carrier,

figure 5 shows the data processing apparatus incorporated in a transmission apparatus for transmitting the residual bitstream signal via a transmission medium,

figure 6 shows a further embodiment of the recording apparatus, further provided with an error correction encoder and a channel encoder,

figure 7 shows an embodiment of another data processing apparatus for reconverting the residual bitstream signal into a replica of the original audio signal,

figure 8 shows an embodiment of the signal combination unit and the prediction unit incorporated in the apparatus of figure 7,

figure 9 shows the data processing apparatus of figure 7 incorporated in a reproducing apparatus for reproducing the residual bitstream signal from a record carrier, and

figure 10 shows the data processing apparatus of figure 7 incorporated in a receiving apparatus for receiving the residual bitstream signal from a transmission medium,

figure 11 shows a further embodiment of the reproducing apparatus, further provided with a channel decoder and an error correction unit,

figure 12 shows the derivation of a conversion table for another embodiment of the prediction unit in the apparatus of figure 1,

figure 13 shows another embodiment of the data processing apparatus,

figure 14 shows an embodiment of a data processing apparatus for reconverting the residual bitstream signal obtained by the apparatus of figure 14 into a replica of the original audio signal,

figure 15 shows the application of a data compression unit in a recording apparatus,

figure 16 shows the application of a data expansion unit in a reproduction apparatus,

figure 17a shows the frequency spectrum of the output signal of the 1-bit A/D converter of figure 1, and figure 17b shows the frequency spectrum of the same output signal in a smaller frequency range,

figure 18 shows a modification of the apparatus of figure 1,

figure 19 a data processing apparatus provided with an arithmetic coder, and

figure 20 a data processing apparatus provided with an arithmetic decoder.

Figure 1 shows an embodiment of the data processing apparatus in accordance with the invention, comprising an input terminal 1 for receiving the audio signal. In the present example, the audio signal is an analog audio signal. The input terminal 1 is coupled to an input 2 of a 1-bit A/D converter 4, also called: sigma-delta modulator. An output 6 of the 1-bit A/D converter 4 is coupled to an input 8 of a prediction unit 10 as well as to a first input 40 of a signal combination unit 42. An output 12 of the prediction unit 10 is coupled to a second input 44 of the signal combination unit 42, an output 48 of which is coupled to an output terminal 14.

The 1-bit A/D converter 4 is adapted to carry out a 1-bit A/D conversion on the audio signal so as to obtain a bitstream signal which is supplied to the output 6. To that purpose, the A/D converter 4 receives a sampling frequency equal to $N.f_s$ via an input 16. f_s is a frequency equal to eg. 32 kHz, 44.1 kHz or 48 kHz and N is a large number, such as 64. The audio signal is sampled in the A/D converter 4 with a sampling frequency of eg. 2.8224 MHz (64 x 44.1 kHz). The bitstream signal appearing at the output 6 of the A/D converter thus has a bitrate of 2.8224 MHz.

The prediction means 10 are adapted to carry out a prediction step on the bitstream signal applied to its input 8 so as to obtain a predicted bitstream signal at its output 12. The signal combination means 42 is adapted to combine the bitstream signal applied to its input 40 and the predicted bitstream signal applied to its input 44 so as to obtain a residue bitstream signal which is supplied to its output 14.

Figure 17a shows a frequency spectrum of the bitstream signal present at

the output 6 of the A.D converter 4, for an input signal in the form of a 5 kHz sinusoid, sampled with a sampling frequency of 2.8224 MHz. The spectrum thus shows frequencies between 0 Hz and 1.4 MHz. Figure 17b shows part of the spectrum shown in figure 17a, namely that part between 0 Hz and 100 kHz, so as to more clearly show the 5 kHz sinusoid comprised in the bitstream signal. Clearly visible is the noise-like character of the bitstream signal, especially in the higher frequency region, which seems to imply that carrying out a prediction step on the said signal, with a subsequent signal combination of the predicted version of the bitstream signal and the bitstream signal so as to obtain said residual signal will not result in a substantial amount decrease in entropy of the residual signal, such decrease of entropy of the residual signal, compared to the input signal of the prediction unit being the general aim of a prediction unit.

Contrary to this, investigations have made clear that a significant decrease in entropy of the residual bitstream signal can be obtained by carrying out a prediction step, in spite of the noisy-like character of the bitstream signal.

The prediction unit 10 can have any form, and could comprise a FIR filter or an IIR filter, where the coefficients of the filter are chosen (or derived) such, that the output signal of the prediction unit 10 is the predicted version of the bitstream signal.

Another embodiment of the prediction unit 10 will be further explained with reference to figure 2 and 3. Figure 2 shows a part of the prediction unit 10, which comprises a three bit shift register 20 having an input coupled to the input 8 of the prediction unit 10. Upon the application of three clock pulses (not shown) to the shift register 20, three subsequent bits x_1,x_2,x_3 of the bitstream signal applied to the input 8 are shifted into the shift register 20. A detector 22 is present having an input 24 coupled to the input 8 of the prediction unit 10. The detector detects the bit value of the next bit x_4 directly following the three subsequent bits x_1,x_2,x_3 in the bitstream signal. Further, a counter 26 is present which counts the number of times that a '0' bit follows a specific three bit bit sequence x_1,x_2,x_3 and the number of times that a '1' bit follows that same specific three bit bit sequence. This is done for all the eight possible 3-bit bit sequences x_1,x_2,x_3.

Explained in a different way. Assume that the three bit sequence '100' is stored in the shift register 20 and that the detector 24 detects the next bit x_4 to be '0'. As a result, the number $N_{4,0}$ in the column 28 is increased by one. Upon the next clock pulse applied to the shift register 20, the 3-bit word stored in the shift register 20 now equals '000'. Assume that the next bit x_4 now equals '1'. As a result, the number $N_{0,1}$ in the column 30 is increased by one.

This procedure is continued for a relatively large portion of the bitstream signal. When the portion of the bitstream signal has been processed in this way, the columns 28 and 29 are filled with numbers $N_{i,0}$,$N_{i,1}$, which indicate the number of occurrences of a '0'-bit or '1'-bit respectively as the next bit following the i-th 3-bit sequence given in column 32, where i runs from 0 to 7 in the present example.

Next, a predicted binary value x_4' is derived from the numbers in the columns 28 and 30 for each of the 3-bit sequences x_1,x_2,x_3 in the column 32, by taking that binary value (either '0' or '1') that resulted in the highest of the count number $N_{i,0}$ and $N_{i,1}$ for the i-th bit sequence in column 32. As an example, if $N_{4,0}$ equals 78 and $N_{4,1}$ equals 532, the predicted bit x_4' in response to the occurrence of the 3-bit bit sequence '100' is chosen equal to '1'. A conversion table can thus be derived comprising the columns 32 and 34, so that for each of the eight possible 3-bit sequences stored in the shift register 20, a corresponding predicted bit x_4' can be generated. In the situation where equal count values $N_{i,0}$ and $N_{i,1}$ have been derived for a three bit bitsequence i, one can choose one of the two binary values '0' or '1' at random as the value for the predicted bit.

It should be noted here, that two counters for each 3-bit bit combination are used to count the numbers of 'zeroes' and 'ones' following said 3-bit bit combination. In spite of this, one could use only one counter which is capable of counting up upon the occurrence of a 'zero' bit following the 3-bit bit combination and counting down in response to the occurrence of a 'one' bit following the 3-bit bit combination. If the count value at the end of the test procedure is higher than at the beginning of the test procedure, the predicted bit will be chosen 'zero'. If the count value appears to be lower than the count value at the beginning of the test procedure, the predicted bit will be chosen 'one'.

If the signal to be processed is substantially time invariant, it may occur that, upon deriving a conversion table from a next portion of the bitstream signal, the same predicted values x_4' will be obtained. In such case, it suffices to derive the conversion table once. For bitstream signals having varying properties, it may be required to each time derive the conversion table from a subsequent portion of the bitstream signal and to predict that portion of the bitstream using its own derived conversion table.

Figure 3 shows a further elaborated version of the prediction unit 10 together with the signal combination unit 42. The input 8 of the prediction unit 10 is coupled to a first input 40 of a signal combination unit 42. An output 46 of the conversion means 26', which comprises the conversion table derived in the way explained above with reference to figure 2, is coupled to a second input 44 of the signal combination unit 42, an output 48

of which is coupled to the output 14 of the data processing apparatus. The signal combination unit 42 can be in the form of an EXOR, but the combination unit 42 may be of a different construction, such as an EXNOR.

In response to a 3-bit bit sequence x_1,x_2,x_3 stored in the shift register 20, the conversion unit 26' supplies the bit x_4' at its output 46. This bit x_4' is a prediction of the bit x_4 present at the inputs of the shift register 20 and the combination unit 42. The combination unit 42 combines the bits x_4 and x_4' so as to obtain a residual bit. Upon a subsequent clock signal (not shown) the bit x_4 present at the input of the shift register 20 is shifted into the shift register 20, so that a new 3-bit bit sequence is stored in the shift register 20. The conversion unit 26' generates a new prediction bit x_4' in response to this new 3-bit bit sequence stored in the shift register 20. The signal combination unit 42 combines this new prediction bit x_4' with the new bit x_4 now present at the input 40 so as to obtain a new residual bit. In this way, a residual bitstream signal is obtained.

Assume that the combination unit 42 is an EXOR, the residual signal has the following property. Assume that both the bits x_4 and x_4' are the same, that is, either '0' or '1'. The residual bit supplied by the EXOR is '0'. Assume now that the bits x_4 and x_4' are not equal to each other. As a result, a '1' bit is generated as a residual bit by the EXOR 42. The occurrence of the '1' bits in the residual signal are thus a measure for the errors between the predicted bitstream signal applied to the input 44 of the combination unit 42 and the bitstream signal applied to the input 40.

Figure 4 shows an embodiment of a recording apparatus comprising the data processing apparatus shown in figure 1, which may include the prediction unit shown in figure 3. The recording apparatus further comprises a data compression unit 150 for data compressing the residual bitstream signal into a data compressed residual bitstream signal and a write unit 50 for writing the data compressed residual bitstream signal in a track on the record carrier 52. In the present example, the record carrier 52 is a magnetic record carrier, so that the write unit 50 comprises at least one magnetic head 54 for writing the residual bitstream signal in the record carrier 52. The record carrier may however be an optical record carrier, such as a CD disk or a DVD disk.

Figure 5 shows an embodiment of a transmitter for transmitting an audio signal via a transmission medium TRM, comprising the data processing apparatus as shown in figure 1, which may include the prediction unit shown in figure 3. The transmitter again comprises the data compression unit 150 and further comprises a transmission unit 60 for applying the data compressed residual bitstream signal to the transmission medium TRM.

The transmission unit 60 could comprise an antenna 62.

Transmission via a transmission medium, such as a radio frequency link or a record carrier, generally requires an error correction encoding and a channel encoding carried out on the data compressed residual signal to be transmitted. Figure 6 shows such signal processing steps carried out on the data compressed residual signal for the recording arrangement of figure 4. The recording arrangement of figure 6 therefore comprise an error correction encoder 56, well known in the art, and a channel encoder 58, also well known in the art.

It has been said above that, in some applications, it suffices to use a fixed conversion table to process the bitstream signal. Upon reconverting the residual bitstream signal into a replica of the original bitstream signal, also a fixed conversion table suffices. In an application where, for subsequent portions of the bitstream signal each time a corresponding conversion table needs to be determined, to generate the residual bitstream signal, it will be required to use the same conversion tables for the portions in question upon reconverting the residual bitstream signal into the replica of the original bitstream signal. In such situation, it may be required to transmit side information representative of the conversion tables used for the various subsequent portions together with the residual signal so as to enable the reconversion upon reception.

As a further example, if it appears that it suffices to use only two conversion tables in the processing apparatus of figure 1, such side information could simply be a selection signal, selecting one of the two conversion tables. A corresponding reconversion apparatus could comprise the two conversion tables as well, and the selection signal could be used to select one of the two conversion tables so as to reconvert the residual bitstream signal into the replica of the original bitstream signal.

It should however be noted that, when having derived a conversion table for a portion of the bitstream signal, it is not absolutely necessary to transmit side information corresponding to this conversion table to a reconverter apparatus. The reconverter apparatus may generate the conversion table by itself. The prediction unit in the reconversion apparatus will have a low prediction accuracy in the beginning, but will 'learn' itself so as to obtain a prediction conversion table, which will be substantially identical to the conversion table used in the transmitter apparatus.

Figure 7 shows a schematic embodiment of a second data processing apparatus in accordance with the invention, which is capable of reconverting the residual bitstream signal into the replica of the original bitstream signal. The apparatus has an input

terminal 70 for receiving the residual bitstream signal, as supplied by the data processing apparatus of figure 1. The input terminal 70 is coupled to a first input 86 of a signal combination unit 88, which has an output 76 coupled to an input 72 of a prediction unit 74 as well as to an input 78 of a 1-bit D/A converter 80. An output 98 of the prediction unit 74 is coupled to a second input 101 of the signal combination unit 88. An output 82 of the D/A converter 80 is coupled to an output terminal 84.

The apparatus of figure 7 receives the residual bitstream via its input 70, which is supplied to the input 86 of the signal combination unit 88. The signal combination unit 88 combines the residue bitstream signal received via its input 86 with a predicted bitstream signal received via its input 101 so as to obtain a reconverted bitstream signal, and to supply the reconverted bitstream signal to its output 76. The prediction unit 74 carries out a prediction step on the reconverted bitstream signal so as to obtain said predicted bitstream signal at its output 98. The D/A converter unit 80 carries out a D/A conversion on the reconverted bitstream signal so as to obtain the replica of the original audio signal, which is supplied to the output terminal 84.

The prediction unit 74 can have any form, and could comprise a FIR filter or an IIR filter, where the coefficients of the filter are chosen (or derived) such, that the output signal of the prediction unit 74 is the predicted version of the bitstream signal.

Another embodiment of the prediction unit 74 will be further explained with reference to figure 8. The input 72 of the prediction unit 74 is coupled to an input 92 of a three bit shift register 94. The three outputs of the three bit positions in the shift register 94 are coupled to corresponding inputs of a conversion unit 96. The conversion unit 96 comprise the conversion table discussed and explained above with reference to the figures 2 and 3. An output 98 of the conversion unit 96 is coupled to a second input 101 of the signal combination unit 88. The signal combination unit 88 can be in the form of an EXOR, but the combination unit 88 may be of a different construction, such as an EXNOR. It will be clear that, if the signal combination unit 42 of figure 3 is an EXOR, the signal combination unit 88 of figure 8 must be an EXOR as well, in order to regenerate a replica of the original bitstream signal.

In response to a 3-bit bit sequence x_1,x_2,x_3 stored in the shift register 94, the conversion unit 96 supplies the bit x_4' at its output 98, in the way explained above with reference to the figures 2 and 3. This bit x_4' is a prediction of the bit x_4 that will be supplied upon the next clock pulse by the combination unit 88 and stored as the new bit x_3 in the most right storage position of the shift register 94. The residual bit present at the input 86 of the

combination unit 88 is combined with the predicted bit x_4' so as to obtain the replica of the original bit x_4 in the original bitstream signal. When the residual bit is '0', which meant that a correct prediction was carried out in the apparatus of figure 1 and 3, the combination of the residual bit with the predicted bit x_4' results in the bitvalue of the bit x_4' to appear at the output 90 of the combination unit 88. When the residual bit is '1', which meant that an incorrect prediction was carried out in the apparatus of figure 1 and 3, the combination of the residual bit with the predicted bit x_4' results in the inverse bitvalue of the bit x_4' to appear at the output 90 of the combination unit 88. In both cases, a correct replica of the bit x_4 will appear at the output 76 of the combination unit 88.

Upon a subsequent clock signal (not shown) the bit x_4 present at the input of the shift register 94 is shifted into the shift register 94, so that a new 3-bit bit sequence is stored in the shift register 94. The conversion unit 96 generates a new prediction bit x_4' in response to this new 3-bit bit sequence stored in the shift register 94. The signal combination unit 88 combines this new prediction bit x_4' with the next residual bit in the residual bitstream signal applied to the input 86 so as to obtain a replica of the next bit x_4 in the bitstream signal. In this way, the replica of the bitstream signal is obtained.

Figure 9 shows the data processing apparatus of figure 7 incorporated in a reproduction apparatus. The reproducing apparatus further comprises a data expansion unit 162 for data expanding the data compressed residual bitstream signal so as to obtain a replica of the original residual bitstream signal and a read unit 100 for reading the data compressed residual bitstream signal from a track on the record carrier 52. In the present example, the record carrier 52 is a magnetic record carrier, so that the read unit 100 comprises at least one magnetic head 102 for reading the data compressed residual bitstream signal from the record carrier 52. The record carrier may however be an optical record carrier, such as a CD disk or a DVD disk.

Figure 10 shows an embodiment of a receiver for receiving an audio signal via a transmission medium TRM, comprising the data processing apparatus as shown in figure 7. The receiver further comprises the data expansion unit 162 and a receiving unit 105 for receiving the data compressed residual bitstream signal from the transmission medium TRM. The receiving unit 105 could comprise an antenna 107.

As has been explained above, transmission via a transmission medium, such as a radio frequency link or a record carrier, generally requires an error correction encoding and a channel encoding carried out on the data compressed residual signal to be transmitted, so that a corresponding channel decoding and error correction can be carried out

upon reception. Figure 11 shows the signal processing steps of channel decoding and error correction carried out on the received signal, received by the reading means 100 for the reproducing arrangement of figure 9. The reproducing arrangement of figure 11 therefore comprise a channel decoder 110, well known in the art, and an error correction unit 112, also well known in the art, so as to obtain a replica of the data compressed residual bitstream signal.

It has also been said above that, in some applications, it suffices to use a fixed conversion table to process the bitstream signal in the apparatus of the figures 1 and 3. Upon reconverting the residual bitstream signal into a replica of the original bitstream signal, also a fixed conversion table suffices, so that no side information needs to be transmitted to the processing apparatus of the figures 7 and 8. In an application where, for subsequent portions of the bitstream signal each time a corresponding conversion table needs to be determined in the apparatus of the figures 1 and 3, to generate the residual bitstream signal, it will be required to use the same conversion tables for the portions in question upon reconverting the residual bitstream signal into the replica of the original bitstream signal in the apparatus of the figures 7 and 8. In such situation, it will be required to transmit side information representative of the conversion tables used for the various subsequent portions together with the residual signal so as to enable the reconversion upon reception. As an example, this side information thus needs to be recorded on the record carrier 52, such as in the application where the apparatus of the figures 1 and 3 is accommodated in a recording apparatus and the apparatus of the figures 7 and 8 is incorporated in a reproducing apparatus of the figure 9 or 11, and be reproduced from said record carrier upon reproduction.

If it appears that it suffices to use only two conversion tables in the processing apparatus of figure 1, such side information could simply be a selection signal, selecting one of the two conversion tables. A corresponding reconversion apparatus could comprise the two conversion tables as well, and the selection signal could be used to select one of the two conversion tables so as to reconvert the residual bitstream signal into the replica of the original bitstream signal.

The embodiments described above are based on the prediction of 1 bit (x_4') following a sequence of three subsequent bits (x_1,x_2,x_3) in the bitstream signal. In general, the prediction unit can be capable of predicting from n subsequent bits in the bitstream signal m prediction bits, said m prediction bits being predicted versions of m subsequent bits in the bitstream signal following said n subsequent bits in the bitstream signal, where n and m are integers larger than zero.

Figure 12 shows an example how to derive a conversion table which is capable of predicting one or two prediction bits from a sequence of four consecutive bits x_1,x_2,x_3,x_4 in the bitstream signal. Figure 12 shows a part of another prediction unit 10', which comprises a four bit shift register 20' having an input coupled to the input 8 of the prediction unit 10'. Upon the application of four clock pulses (not shown) to the shift register 20', four subsequent bits x_1,x_2,x_3,x_4 of the bitstream signal applied to the input 8 are shifted into the shift register 20'. A detector 22' is present having an input 24 coupled to the input 8 of the prediction unit 10'. The detector 22' detects the bit value of the next two bits x_5,x_6 directly following the four subsequent bits x_1,x_2,x_3,x_4 in the bitstream signal. Further, a counter 26'' is present which counts the number of times that a '0' bit follows a specific four bit bit sequence x_1,x_2,x_3,x_4, the number of times that a '1' bit follows that same specific four bit bit sequence, the number of times that a two bit bitsequence '00' follows that same specific four bit bit sequence x_1,x_2,x_3,x_4, the number of times that a two bit bitsequence '01' follows that same specific four bit bit sequence, the number of times that a two bit bitsequence '10' follows that same specific four bit bit sequence x_1,x_2,x_3,x_4 and the number of times that a two bit bitsequence '11' follows that same specific four bit bit sequence. It should be noted here, that the 2-bit bit combination 'b_1,b_2' will be expressed such that the first bit b_1 is the bit x_5, where the second bit b_2 is the bit x_6.

Suppose that the detector 22' has detected that the two bits x_5,x_6 equal '01'. As a result, the counter 26'' increases the count value $N_{i,0}$ in the column 28' by one and the count value $N_{i,3}$ in the column 30' by one, where i runs from 0 to 15 and corresponds to the i-th four bit bitsequence given in the column 32' of the table in figure 12.

Next, upon the application of a number of P clock pulses to the apparatus of figure 12, where P need not necessarily be equal to 2, but may be larger, another 4-bit bitsequence x_1,x_2,x_3,x_4 of the bitstream signal is stored in the shift register 20'. The detector 22' detects the bit values of the next two bits x_5,x_6 in the bitstream signal following the said 4-bit bitsequence. Suppose, the next two bits equal '11'. As a result, the counter 26'' increases the count value $N_{i,1}$ in the column 29 by one and the count value $N_{i,5}$ in the column 31 by one, where i corresponds to the four bit bitsequence stored in the shift register 20', which is assumed to be the i-th four bit bitsequence given in the column 32' of the table in figure 12.

This procedure is repeated a plurality of times, so that for all the sixteen possible 4-bit bit sequences x_1,x_2,x_3,x_4 the count values $N_{i,0}$ to $N_{i,5}$ have been obtained. The count values $N_{i,0}$ to $N_{i,5}$ indicate the number of occurrences of the one bit and two bit

bitsequences following the i-th 4-bit sequence given in column 32'.

Next, either a predicted binary value x_5' or a predicted 2 bit binary sequence $x_5'x_6'$ is derived, based upon the count values in the columns 28', 29, ... to 31, for each of the 4-bit sequences x_1,x_2,x_3,x_4 in the column 32.

Suppose that the count value $N_{i,0}$ or the count value $N_{i,1}$ of the six count values $N_{i,0}$ to $N_{i,5}$ for the i-th 4 bit bitsequence in column 32' is substantially larger than all the others. In such situation, one can decide to choose the '0' bit or '1' bit, respectively, as the prediction bit x_5'. Suppose that $N_{i,0}$ and $N_{i,2}$ do not differ very much and are larger than the other four count values.In such situation, one could decide to choose the bit combination '00' as the prediction bits x_5',x_6' for the i-th bitsequence. In this way, the conversion table obtained can thus comprise a column 33 which may comprise either a one bit value as a prediction bit for predicting the bit following a specific 4-bit bit sequence in the bitstream signal, or a 2-bit binary word as a 2-bit prediction word for predicting the 2-bit word following another specific 4-bit bit sequence in the bitstream signal.

Figure 13 shows schematically another embodiment of the data processing apparatus for data processing an audio signal, which comprises a conversion unit 130 in the form of a conversion table, such as the one explained with reference to figure 12. That means that the conversion table comprises the columns 32' and 33 given in figure 12, so that upon the receipt of a specific 4-bit bit sequence x_1,x_2,x_3,x_4, as given in column 32', a specific prediction bit x_5 or two specific prediction bits x_5,x_6 will be generated at the output 131 of the conversion unit 130.

The functioning of the apparatus of figure 13 is as follows. In response to a specific 4-bit bitsequence stored in the shift register 20' the conversion unit 130 generates, as an example a one bit word, equal to '1'. This is the case when a 4-bit sequence '0000' is stored in the shift register 20'. The column 33 shows that upon such 4-bit sequence, see column 32' in the table of figure 12, a '1' bit is predicted, see the column 33 in the table of figure 12. The predicted bit x_5' is supplied to the input 44 of the combination unit 42 in which the predicted bit x_5' is combined with the real bit x_5 in the bitstream present at the input 40. Next, upon one clock pulse, generated by a central processing unit 132, the information in the shiftregister 20' is shifted one position to the left, so that the bit x_5 is now stored in the most right storage location of the shift register 20'. Suppose, this bit was indeed a '1' bit, as predicted.

Next, the conversion unit converts the 4-bit sequence '0001' stored in the shift register 20' into a 2-bit word '01', see the columns 32' and 33 in the table of figure 12,

which 2-bit word is supplied to the output 131. The central processing unit 132 now generates two clock pulses so that the 2-bit prediction word '01' can be combined in the combination unit 42 with the actual bits x_5,x_6 in the bitstream signal. The two clock pulses also result in a shift by two positions to the left in the shift register 20' so that the shift register has the values '0' and '1' stored in the positions in the shift register 20', indicated by x_1 and x_2, and the actual bits x_5 and x_6 mentioned above are now stored as the new bits x_3 and x_4 in the shift register 20'. Thus, upon predicting one bit, the central processing unit 132 generates one clock pulse, after which a subsequent prediction step is carried out, whereas, upon predicting a 2-bit word, the central processing unit 132 generates two clock pulses before a subsequent prediction step is carried out.

Suppose that, for subsequent portions of the bitstream signal, a corresponding conversion table is derived first, eg. in the way explained above with reference to figure 12, it is desired to transmit the conversion table together with the residual bitstream signal so as to enable reconversion upon reception of the residual bitstream signal. Figure 13 shows a connection 135 between the prediction unit 26''' and the central processing unit 132. Via this connection, the conversion table derived in the way described with reference to figure 12 can be supplied to the central processing unit 132 and subsequently supplied to an output 137 for transmission together with the residual bitstream signal via the transmission medium

Figure 14 shows a corresponding apparatus for reconverting the residual bitstream signal supplied by the apparatus of figure 13. The apparatus of figure 14 shows a large resemblance with the apparatus of the figures 7 and 8, in the sense that the signal combination unit 88 and the D/A converter 80 are the same as the a signal combination unit and the D/A converter respectively of figure 7. The input 72 of the prediction unit 74' is coupled to an input 92 of a four bit shift register 94'. The four outputs of the four bit positions in the shift register 94' are coupled to corresponding inputs of a conversion unit 96'. The conversion unit 96' comprise the conversion table discussed and explained above with reference to the figure 12. An output 98 of the conversion unit 96' is coupled to a second input 101 of the signal combination unit 88.

In response to a 4-bit bitsequence x_1,x_2,x_3,x_4 stored in the shift register 94', the conversion unit 96' supplies either a 1-bit x_5' at its output 98 or a 2-bit word x_5',x_6', in the way explained above with reference to figure 12. This bit x_5' is a prediction of the bit x_5, given by the conversion table 96', that will be supplied upon the next clock pulse by the combination unit 88 and stored as the new bit x_4 in the most right storage

position of the shift register 94'. The residual bit present at the input 86 of the combination unit 88 is combined with the predicted bit x_5' upon the clock pulse generated by the central processing unit 140, so as to obtain the replica of the original bit x_5 in the original bitstream signal. When the residual bit is '0', which meant that a correct prediction was carried out in the apparatus of figure 13, the combination of the residual bit with the predicted bit x_5' results in the right of the bit x_5' to appear at the output 90 of the combination unit 88 as the bit x_5. When the residual bit is '1', which meant that an incorrect prediction was carried out in the apparatus of figure 13, the combination of the residual bit with the predicted bit x_5' results in the inverse right of the bit x_5' to appear at the output 90 of the combination unit 88 as the bit x_5. In both cases, a correct replica of the bit x_5 will appear at the output 76 of the combination unit 88.

The 2-bit prediction x_5',x_6' is a prediction of the 2-bit word x_5,x_6, generated by the conversion table 96', that will be supplied upon the next two clock pulses of the central processing unit 140 by the combination unit 88 and stored as the new 2-bit word x_3,x_4 in the two most right storage positions of the shift register 94'. Two residual bits present at the input 86 of the combination unit 88 are combined with the predicted 2-bit word x_5',x_6' so as to obtain the replica of the original 2-bit word x_5,x_6 in the original bitstream signal. When the two residual bits are '0,0', which meant that a correct prediction was carried out in the apparatus of figure 13, the combination of the residual bits with the predicted bits x_5',x_6' results in the right of the two bits x_5',x_6' to appear at the output 90 of the combination unit 88 as the bits x_5,x_6. When the residual bits were '1,1', which meant that an incorrect prediction was carried out in the apparatus of figure 13 on both the bits x_5 and x_6, the combination of the two residual bits with the predicted bits x_5',x_6' results in the inverse bitvalues of the bits x_5',x_6' to appear at the output 90 of the combination unit 88 as the bits x_5,x_6. When one of the two residual bits is '1' and the other is '0', this means that one of the prediction bits is wrong and should be inverted in order to obtain two correct bits x_5,x_6. In all cases, a correct replica of the 2-bit word x_5,x_6 will appear at the output 76 of the combination unit 88.

In the situation where, for subsequent portions of the bitstream signal, a corresponding conversion table is derived first in the apparatus of figure 13, eg. in the way explained above with reference to figure 12, it is desired to transmit the conversion table together with the residual bitstream signal so as to enable reconversion upon reception of the residual bitstream signal in the apparatus of figure 14. Figure 14 therefore shows an input terminal 142 for receiving the conversion table. The input terminal 142 is coupled to the

central processing unit 140, which has a connection 144 with the prediction unit 96'. Via this connection, the conversion table can be supplied to the prediction unit 96'.

It has been said earlier that a data compression step is carried out on the residual bitstream signal prior to transmission. Preferably, a data compression using a lossless coder is carried out. Lossless coders have the advantage that they can data compress the audio signal in such a way that, after data expansion by a lossless decoder, the original audio signal can be reconstructed in a substantially lossless way. That means that there is substantially no loss of information after compression-expansion. Lossless coders can be in the form of a variable length coder. Variable length coders are well known in the art. Examples of such variable length coders are Huffman coders, arithmetic coders and Lempel-Ziv coders. Reference is made in this respect to the publications 'A method for the construction of minimum-redundancy codes' by D.A. Huffman, document D4 in the list of related documents, 'An introduction to arithmetic coding' by G.G. Langdon, document D5 in the list of related documents, and 'A universal algorithm for sequential data compression' by J. Ziv et al, document D6 in the list of related documents.

Figure 15 shows an embodiment in which the apparatus of figure 1 is followed by a data compression unit 150, such as a lossless coder. The data compressed residual bitstream signal is recorded on an optical record carrier 156 by means of an optical recording unit 154.

Figure 16 shows the corresponding reproduction from the optical record carrier 156. The apparatus shown in figure 16 comprises a data expansion unit 162, such as a lossless decoder, that carries out a data expansion step on the data compressed residual bitstream signal. The regenerated residual bitstream signal is supplied to the input 70 of the apparatus of figure 7.

A further modification of the embodiment of figure 1 is as follows. In this modification, the prediction unit 10 is coupled between the output of the signal combination unit 42 and the input 44 of the signal combination unit 42. In this modification, the predicted version of the bitstream signal is derived by the prediction unit from the residual signal, supplied by the signal combination unit 42. This modification is shown in figure 18, which is in fact identical to the circuit construction of the prediction unit and the signal combination unit shown in figure 7.

In an equivalent way, a further modification of the embodiment of figure 7 is as follows. In this modification, the prediction unit 74 is coupled between the input terminal 70 and the input 101 of the signal combination unit 88. In this modification, the predicted

version of the bitstream signal is derived by the prediction unit from the residual signal, supplied to the processing apparatus via the terminal 70. This modification is in fact identical to the circuit construction of the prediction unit and the signal combination unit shown in figure 1.

A further improvement of the data processing apparatus can be obtained by a specific embodiment of the prediction unit, such as the prediction unit 10 in figure 1. In this specific embodiment, the prediction unit 10 is provided with an integrator for integrating the input signal, which is a representation of the bitstream signal, in the sense that the input signal has -1 and +1 representation values to represent the '0' and '1' bits in the bitstream signal. The integrator simply sums all the representation values, so its instantaneous output is the cumulative sum of all -1 and +1 values it has received. What the prediction unit in fact does, is to generate a pseudo audio signal and the predicted bit for the bitstream signal to be supplied to the output 12 is derived from this pseudo audio signal in the following way.

The predictor derives from the last n sample values of the pseudo audio signal generated by the integrator a prediction value for the next sample of the pseudo audio signal. Next the value of the last sample of the pseudo audio signal generated is compared with the predicted value of the next sample. If, viewed along an amplitude axis, the value of the last sample of the pseudo audio signal is smaller than the prediction value of the next sample, it is concluded that the next predicted bit in the predicted bitstream signal corresponds to the +1 value (or logical '1') and when the value of the last sample of the pseudo audio signal is larger than the prediction value of the next sample, it is concluded that the next predicted bit in the bitstream signal corresponds to the -1 value (or logical '0'). The predicted bits are supplied to the output of the prediction unit 10 as the predicted bitstream signal.

The predicted value of the next sample can be obtained by approximating the last n (which eq equals 40) samples of the pseudo audio signal with a straight line. It will be understood that more sophisticated approximation procedures (filter techniques) are equally well possible to predict the next sample value. In such situation, as said earlier, filter coefficients for such filters should be derived for the signal on a frame basis and transmitted so as to enable a corresponding decoding on the receiver side.

Another data processing apparatus is shown in figure 19. In the data processing apparatus of figure 19, the bitstream signal is supplied to the input 44 of the signal combination unit 42, and via a prediction filter 10' and a quantizer Q to the input 40 of the signal combination unit 42. The apparatus is further provided with a data compression unit 150' which comprises an entropy encoder 154 and a probability determining unit 156. In the

present example, the entropy encoder 154 is in the form of an arithmetic coder for encoding the residual bitstream signal into a data compressed residual bitstream signal in response to probability values p supplied to its input 192. The probability determining unit 156 determines a probability value indicating the probability that a bit in the residual bitstream signal supplied by the combination unit 42 has a predetermined logical value, such as '1'. This probability value, denoted p in figure 19, is supplied to the arithmetic coder 154 so as to enable the data compression of the residual bitstream signal in the arithmetic coder 154. The determining unit 156 determines this probability value from the output signal of the prediction filter 10'. This is different from what one would expect when using an arithmetic coder in the data compression unit 150, such as in figure 4 or 15, for compressing the residual bitstream signal. When using an arithmetic coder in the compression unit 150, the probability unit 156 would derive the probability value from the residual bitstream signal itself. In the embodiment of figure 19, however, the probability determining unit 156 derives the probability value from the output signal generated by the prediction filter 10'. This has an advantage, in that a higher compression ratio can be obtained with the arithmetic coder 154. The arithmetic coder 154 can data compress the residual bitstream signal on a frame basis.

The functioning of the apparatus of figure 19 is as follows. The prediction filter 10' realizes a prediction filtering on the bitstream signal so as to obtain a multi bit output signal. The multi bit output signal has a plurality of levels within a range of eg. +3 and -3. A quantizer Q receives the multi bit output signal and generates a bitstream signal therefrom, eg. by allocating a bit of '1' logical value if the multi bit output signal has a positive value and allocating a bit of '0' logical value if the multi bit output signal has a negative value. Further, for each of a plurality of subintervals in the value range of the multi bit output signal, it is determined what the probability is that the corresponding bit in the residual signal is eg. a '1' bit. This can be realized by counting the number of 'ones' and 'zeroes' occurring in the residual bitstream signal during a specific time interval, when the multi bit output signal falls in one of such ranges. The probabilities thus obtained for the various values in the multi bit output signal is subsequently supplied as the probability signal p to the arithmetic coder 154. The data compressed residual bitstream signal is supplied by the arithmetic coder 154 to an output line 158, for transmission via a transmission medium TRM.

Figure 20 shows a corresponding data processing apparatus for decoding the data compressed residual bitstream signal, received via the transmission medium TRM. The

data processing apparatus of figure 20 comprises an entropy decoder 172, which receives the data compressed residual bitstream signal via an input 174. In the present example, the entropy decoder 172 is in the form of an arithmetic decoder that carries out an arithmetic decoding step on the data compressed bitstream signal under the influence of a probability signal p, supplied to an input 176 so as to generate a replica of original residual bitstream signal which is supplied to an output 178. The replica is supplied to an input 86 of the signal combination unit 88. The signal combination unit 88 further receives a predicted version of the bitstream signal via the input 101 and generates the replica of the original bitstream signal at its output 76. The output 76 is coupled via a prediction filter 74'and a quantizer Q to the input 101 of the signal combination unit 88. The functioning of the prediction filter 74' and the quantizer Q can be identical to the functioning of the prediction filter 10' and the quantizer Q in figure 19, that is: the prediction filter 74' derives its filter coefficients from the input signal it receives via its input 72. In another embodiment, the prediction filter 74' receives the filter coefficients from side information received via the transmission medium TRM from the encoder apparatus of figure 19, as will be explained below.

Further, a probability supply unit 180 is present for supplying the probability signal p to the arithmetic decoder 172. The probability signal p can be obtained in different ways. One way is, to derive the probability signal p from the output signal of the prediction filter 74', in the same way as the probability determining unit 156 determines then probability signal p from the prediction filter 10' in figure 19. In such situation, the supply unit 180 in figure 20 can be identical to the determining unit 156 in figure 19, and the supply unit 180 has an input coupled to the output of the prediction filter 74'. Another way of generating the probability signal p, is by using side information received via the transmission medium TRM, as will be explained hereafter.

Side information can be generated by the apparatus of figure 19 for transmission to the apparatus of figure 20. Such side information can include the filter coefficients for the filter 10' that are determined on a frame by frame basis, which coefficients are transmitted to the filter 74' for setting the correct filter characteristic of the filter 74'. Further, the apparatus of figure 19 can generate parameters that describe the conversion of the multi bit output signal of the prediction filter 10' into the probability signal p. Such parameters are also included in the side information and transmitted to the supply unit 180, so as to enable the regeneration of the probability signal p in the apparatus of figure 20.

In the above described embodiments of the figures 19 and 20, it is explained

how the probability signal p can be derived from the multi bit output signal from the prediction filter 10' and 74' respectively. It should however be noted that the application of an arithmetic coder is also possible in data processing apparatuses that derive the predicted signal in a different way. Reference is made in this respect to the embodiments shown in figure 1, where the prediction unit 10 is in the form as disclosed in the figures 2 or 12. Now another way of deriving the probability signal p is required. It will be clear that, in the embodiments of the prediction unit as shown in figures 2 and 12, the probability signal p can be derived from the count numbers derived in the detector 22 and 22' respectively.

The entropy encoder used in the embodiment of figure 19 is adapted to encode the residual bitstream signal using a probability signal in order to obtain the data compressed residual bitstream signal. One of such entropy encoder is the arithmetic coder described above. One other type of such entropy coder is, as an example, the well known finite state coder. The entropy decoder used in the embodiment of figure 20 is adapted to decode the data compressed residual bitstream signal using a probability signal in order to obtain a replica of the residual bitstream signal. One of such entropy decoder is the arithmetic decoder described above. One other type of such entropy decoder is, as an example, the well known finite state decoder.

Whilst the invention has been described with reference to preferred embodiments thereof, it is to be understood that these are not limitative examples. Thus, various modifications may become apparent to those skilled in the art, without departing from the scope of the invention, as defined by the claims. When the audio signal is supplied in digital form, such as sampled at 44.1 kHz and the samples being expressed in eg. 16 bits, the A/D converter means are adapted to oversample the digital audio signal with eg. the frequency of 64 x 44.1 kHz so as to obtain the 1-bit bitstream signal which is supplied to the prediction unit 10.

Further, as regards the conversion tables, such as the one shown and described in figure 12, the following can be said. In the phase of deriving the conversion table, it may occur that, as an example, the count values are such that the bit sequences 0,0,0,0 and 0,0,1,0 result in the same prediction bit(s), that the bit sequences 0,0,0,1 and 0,0,1,1 result in the same prediction bit(s), that the bit sequences 0,1,0,0 and 0,1,1,0 result in the same prediction bit(s), that the bit sequences 1,0,0,0 and 1,0,1,0 result in the same prediction bit(s), the bit sequences 1,1,0,0 and 1,1,1,0 result in the same prediction bit(s), that the bit sequences 1,0,0,1 and 1,0,1,1 result in the same prediction bit(s), that the bit sequences 1,1,0,1 and 1,1,1,1 result in the same prediction bit(s), and that the bit sequences 0,1,0,1

and 0,1,1,1 result in the same prediction bit(s). In this situation, the bit x_3 is in fact a don't care bit and the prediction bit(s) x_4 or x_4,x_5 can be predicted from the bit combination x_1,x_2,x_4 alone.

Further, the invention lies in each and every novel feature or combination of features.

List of related documents

(D1) EP-A 402,973 (PHN 13.241)

(D2) 'A digital decimating filter for analog-to-digital conversion of hi-fi audio signals', by J.J. van der Kam in Philips Techn. Rev. 42, no. 6/7, April 1986, pp. 230-8

(D3) 'A higher order topology for interpolative modulators for oversampling A/D converters', by Kirk C.H. Chao et al in IEEE Trans. on Circuits and Systems, Vol 37, no. 3, March 1990, pp. 309-18

(D4) 'A method for the construction of minimum-redundancy codes', by D.A. Huffman in Proc. of the IRE, Vol. 40(10), September 1952.

(D5) 'An introduction to arithmetic coding' by G.G. Langdon, IBM J. Res. Develop., Vol. 28(2), March 1984.

(D6) 'A universal algorithm for sequential data compression' by J. Ziv et al, IEEE TRans. on Inform. Theory, Vol. IT-23, 1977.

(D7) EP patent application no. 96202807.2, filing date 10-10-96 (PHN 16.029)

Claims

1. Data processing apparatus for data processing an audio signal, the data processing apparatus comprising

- input means for receiving the audio signal,
- conversion means for carrying out a conversion on the audio signal so as to obtain a 1-bit bitstream signal, the conversion means comprising sigma-delta modulator means,
- prediction means for carrying out a prediction step on a signal so as to obtain a predicted bitstream signal,
- signal combination means for combining the bitstream signal and the predicted bitstream signal so as to obtain a residual bitstream signal, and
- output means for supplying the residual bitstream signal.

2. Data processing apparatus as claimed in claim 1, wherein the audio signal is an analog audio signal and the conversion means comprising A/D conversion means for carrying out a 1-bit A/D conversion on the analog audio signal so as to obtain said bitstream signal.

3. Data processing apparatus as claimed in claim 2, wherein said A/D conversion means is a sigma-delta modulator.

4. Data processing apparatus as claimed in claim 1, 2 or 3, wherein the prediction means comprise a predictor unit for predicting from n subsequent bits in the bitstream signal m prediction bits, said m prediction bits being predicted versions of m subsequent bits in the bitstream signal following said n subsequent bits in the bitstream signal, where n and m are integers larger than zero.

5. Data processing apparatus as claimed in claim 4, wherein the signal combination means are adapted to combine the m prediction bits with said m subsequent bits in the bitstream signal so as to obtain m subsequent bits of the residual bitstream signal.

6. Data processing apparatus as claimed in claim 5, wherein the signal combination means comprise an EXOR gate.

7. Data processing apparatus as claimed in claim 4, 5 or 6, wherein the prediction means comprise a conversion table for supplying m prediction bits in response to a

sequence of n bits from the bitstream signal.

8. Data processing apparatus as claimed in claim 7, where the conversion table is adapted to supply m_1 prediction bits for a first sequence of n bits of the bitstream signal and m_2 prediction bits for a second sequence of n bits in the bitstream signal, where m_1 and m_2 are integers that are not equal to each other.

9. Data processing apparatus as claimed in anyone of the claims 4 or 8, wherein the prediction means comprise calculation means for determining for a portion of the bitstream signal those sequence of m bits following a predetermined sequence of n subsequent bits of the bitstream signal that has the highest probability of occurrence after the occurrence of said predetermined sequence of n bits in the bitstream signal, and allocating means for allocating that sequence of m bits as the m prediction bits to the predetermined sequence of n bits.

10. Data processing method for data processing an audio signal, the data processing method comprising the steps of

- receiving the audio signal,
- carrying out a conversion on the audio signal so as to obtain a 1-bit bitstream signal, the conversion step comprising a sigma-delta modulation step,
- carrying out a prediction step on a signal so as to obtain a predicted bitstream signal,
- combining the bitstream signal and the predicted bitstream signal so as to obtain a residual signal, and
- supplying the residual signal.

11. Transmitter for transmitting an audio signal via a transmission medium, comprising the data processing apparatus as claimed in anyone of the claims 1 to 9, wherein the transmitter further comprises

- data compression means for data compressing the residual bitstream signal so as to obtain a data compressed residual bitstream signal,
- transmission means for applying the data compressed residual bitstream signal to the transmission medium.

12. Transmitter as claimed in claim 11, comprising the data processing apparatus as claimed in claim 7 or 8, wherein the transmission means are further adapted to apply side information representative of a conversion table to the transmission medium.

13. Transmitter as claimed in claim 11, wherein the transmitter further comprises error correction encoding means and/or channel encoding means, for error

correction encoding and/or channel encoding the data compressed residual bitstream signal prior to applying the residual bitstream signal to the transmission medium.

14. Transmitter as claimed in anyone of the claims 11 to 13, wherein the transmitter is in the form of an apparatus for recording an audio signal on a record carrier, and the transmission means is in the form of writing means for writing the residual bitstream signal in a track on the record carrier.

15. Transmitter as claimed in claim 14, wherein the record carrier is an optical or a magnetic record carrier.

16. Record carrier having a residual bitstream signal recorded on it in a track of said record carrier.

17. Data processing apparatus for data processing a residual bitstream signal so as to obtain a replica of an original audio signal, the data processing apparatus comprising

- input means for receiving the residual bitstream signal,
- signal combination means for combining the residual bitstream signal with a predicted bitstream signal so as to obtain a reconverted bitstream signal,
- prediction means for carrying out a prediction step on a signal so as to obtain said predicted bitstream signal,
- D/A conversion means for carrying out a D/A conversion on the reconverted bitstream signal so as to obtain the replica of the original audio signal,
- output means for supplying the replica of the original audio signal.

18. Data processing apparatus as claimed in claim 17, wherein the D/A conversion means comprise a sigma-delta demodulator.

19. Data processing apparatus as claimed in claim 17 or 18, wherein the prediction means comprise a predictor unit for predicting from n subsequent bits in the reconverted bitstream signal m prediction bits, said m prediction bits being predicted versions of m subsequent bits in the reconverted bitstream signal following said n subsequent bits in the reconverted bitstream signal, where n and m are integers larger than zero.

20. Data processing apparatus as claimed in claim 19, wherein the signal combination means are adapted to combine the m prediction bits with m bits in said residual bitstream signal so as to obtain said m subsequent bits of the reconverted bitstream signal.

21. Data processing apparatus as claimed in claim 20, wherein the signal combination means comprise an EXOR gate.

22. Data processing apparatus as claimed in claim 19, 20 or 21, wherein the prediction means comprise a conversion table for supplying m prediction bits in response to a

sequence of n bits from the reconverted bitstream signal.

23. Data processing apparatus as claimed in claim 22, where the conversion table is adapted to supply m_1 prediction bits for a first sequence of n bits of the reconverted bitstream signal and m_2 prediction bits for a second sequence of n bits in the reconverted bitstream signal, where m_1 and m_2 are integers that are not equal to each other.

24. Data processing method for data processing a residual bitstream signal so as to obtain a replica of an original audio signal, the data processing method comprising the steps of

- receiving the residual bitstream signal,
- combining the residual bitstream signal with a predicted bitstream signal so as to obtain a reconverted bitstream signal,
- carrying out a prediction step on a signal so as to obtain said predicted bitstream signal,
- carrying out a D/A conversion on the reconverted bitstream signal so as to obtain the replica of the original audio signal,
- supplying the replica of the original audio signal.

25. Receiver for receiving an audio signal via a transmission medium, comprising the data processing apparatus as claimed in anyone of the claims 18 to 24, wherein the receiver further comprises

- receiving means for retrieving a data compressed residual bitstream signal from the transmission medium,
- data expansion means for data expanding the data compressed residual bitstream signal so as to obtain said residual bitstream signal.

26. Receiver as claimed in claim 25, comprising the data processing apparatus as claimed in claim 22 or 23, wherein the receiving means are further adapted to retrieve side information representative of a conversion table from the transmission medium.

27. Receiver as claimed in claim 25, wherein the receiver further comprises channel decoding means and/or error correction means, for channel decoding and/or error correcting the signal retrieved from the transmission medium so as to obtain said data compressed residual bitstream signal.

28. Receiver as claimed in anyone of the claims 25 to 27, wherein the receiver is in the form of an apparatus for reproducing an audio signal from a record carrier, and the receiving means is in the form of reading means for reading the data compressed residual bitstream signal from a track on the record carrier.

29. Data processing apparatus for data processing a bitstream signal, the data processing apparatus comprising

- input means for receiving a 1-bit bitstream signal,
- prediction means for carrying out a prediction step on a signal so as to obtain a predicted bitstream signal,
- signal combination means for combining the bitstream signal and the predicted bitstream signal so as to obtain a residual bitstream signal, and
- data compression means for data compressing the residual bitstream signal, the data compression means being in the form of an entropy encoder for entropy encoding the residual bitstream signal in response to a probability signal so as to obtain a data compressed residual bitstream signal, the apparatus further comprising probability signal determining means for determining said probability signal from said prediction means, and
- output means for supplying the data compressed residual bitstream signal.

30 Data processing apparatus as claimed in claim 29, wherein the prediction means comprises prediction filter means for carrying out a prediction filter operation on the bitstream signal supplied to its input so as to obtain a multi value output signal and quantizing means for carrying out a quantization step on the multi value output signal so as to obtain the predicted bitstream signal, and wherein the probability determining means are adapted to derive said probability signal from said multi value output signal.

31. Data processing method for data processing a bitstream signal, the data processing method comprising the steps of

- receiving a 1-bit bitstream signal,
- carrying out a prediction step on a signal so as to obtain a predicted bitstream signal,
- combining the bitstream signal and the predicted bitstream signal so as to obtain a residual bitstream signal, and
- data compressing the residual bitstream signal by entropy encoding the residual bitstream signal in response to a probability signal so as to obtain a data compressed residual bitstream signal, the data compression step further comprising the substep of determining said probability signal, and
- supplying the data compressed residual bitstream signal.

32 Data processing method as claimed in claim 31, wherein the prediction step comprises the substeps of carrying out a prediction filter operation on the bitstream signal so

as to obtain a multi value output signal and carrying out a quantization step on the multi value output signal so as to obtain the predicted bitstream signal, and wherein the probability determining substep comprises deriving said probability signal from said multi value output signal.

33. Data processing apparatus for data processing a bitstream signal, the data processing apparatus comprising

- input means for receiving a 1-bit bitstream signal,
- prediction means for carrying out a prediction step on a signal so as to obtain a predicted bitstream signal,
- signal combination means for combining the bitstream signal and the predicted bitstream signal so as to obtain a residual bitstream signal,
- output means for supplying the residual bitstream signal wherein the prediction means comprises integrator means for carrying out an integration operation on the bitstream signal supplied to its input so as to obtain a pseudo audio signal, extrapolation means for deriving an extrapolated sample from the last n samples of the pseudo audio signal generated by the integrator means and derivation means for deriving a next bit value of the predicted bitstream signal from the extrapolated sample and the last sample of the pseudo audio signal generated by the integrator means, where n is an integer value larger than 1.

34. Data processing method for data processing a bitstream signal, the data processing method comprising the steps of

- receiving the a 1-bit bitstream signal,
- carrying out a prediction step on a signal so as to obtain a predicted bitstream signal,
- combining the bitstream signal and the predicted bitstream signal so as to obtain a residual signal, and
- supplying the residual signal, wherein said prediction step comprises the substeps of

- carrying out an integration operation on the bitstream signal received so as to obtain a pseudo audio signal,
- deriving an extrapolated sample from the last n samples of the pseudo audio signal generated in the integration substep,
- deriving a next bit value of the predicted bitstream signal from the extrapolated sample and the last sample of the pseudo audio signal generated in the integration substep, where n is an

integer value larger than 1.

35. Data processing apparatus for data processing a data compressed residual bitstream signal so as to obtain a replica of a bitstream signal, the data processing apparatus comprising

- input means for receiving the data compressed residual bitstream signal,
- data expansion means in the form of an entropy decoder for entropy decoding the data compressed residual bitstream signal in response to a probability signal so as to obtain a replica of said residual bitstream signal,
- means for supplying said probability signal
- signal combination means for combining the residual bitstream signal with a predicted bitstream signal so as to obtain a reconverted bitstream signal,
- prediction means for carrying out a prediction step on a signal so as to obtain said predicted bitstream signal,
- output means for supplying the reconverted bitstream signal.

36. Data processing method for data processing a data compressed residual bitstream signal so as to obtain a replica of a bitstream signal, the data processing method comprising the steps of

- receiving the data compressed residual bitstream signal,
- data expanding the data compressed residual bitstream signal so as to obtain a replica of the residual bitstream signal, the data expansion step comprising the step of carrying out an entropy decoding step on the data compressed residual bitstream signal in response to a probability signal and the step of supplying said probability signal
- combining the residual bitstream signal with a predicted bitstream signal so as to obtain a reconverted bitstream signal,
- carrying out a prediction step on a signal so as to obtain said predicted bitstream signal,
- supplying the reconverted bitstream signal.

37. Data processing apparatus for data processing a residual bitstream signal so as to obtain a replica of a bitstream signal, the data processing apparatus comprising

- input means for receiving the residual bitstream signal,
- signal combination means for combining the residual bitstream signal with a predicted bitstream signal so as to obtain a reconverted bitstream signal,
- prediction means for carrying out a prediction step on a signal so as to obtain

said predicted bitstream signal,

- output means for supplying the reconverted bitstream signal.

wherein the prediction means comprise

- integrator means for carrying out an integration operation on the signal supplied to its input so as to obtain a pseudo audio signal,
- extrapolation means for deriving an extrapolated value from the last n samples of the pseudo audio signal generated by the integrator means,
- derivation means for deriving a next bit value of the predicted bitstream signal from the extrapolated sample and the last sample of the pseudo audio signal generated by the integrator means, where n is an integer value larger than 1.

38. Data processing method for data processing a residual bitstream signal so as to obtain a replica of a bitstream signal, the data processing method comprising the steps of

- receiving the residual bitstream signal,
- combining the residual bitstream signal with a predicted bitstream signal so as to obtain a reconverted bitstream signal,
- carrying out a prediction step on a signal so as to obtain said predicted bitstream signal,
- supplying the reconverted bitstream signal,

wherein the said prediction step comprises the substeps of

- carrying out an integration operation on a bitstream signal so as to obtain a pseudo audio signal,
- deriving an extrapolated sample from the last n samples of the pseudo audio signal generated in the integration substep,
- deriving a next bit value of the predicted bitstream signal from the extrapolated sample and the last sample of the pseudo audio signal generated in the integration substep, where n is an integer value larger than 1.

39. Transmission signal comprising a data compressed residual bitstream signal, which is data compressed by means of a lossless coder.

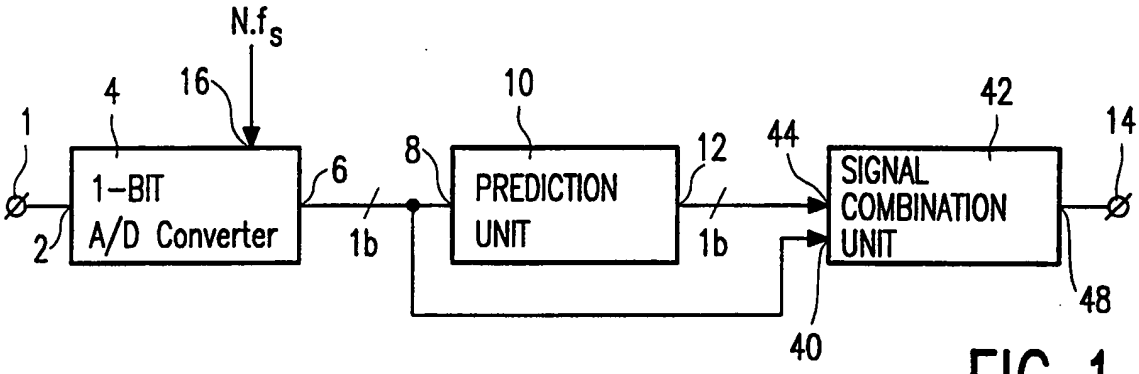

FIG. 1

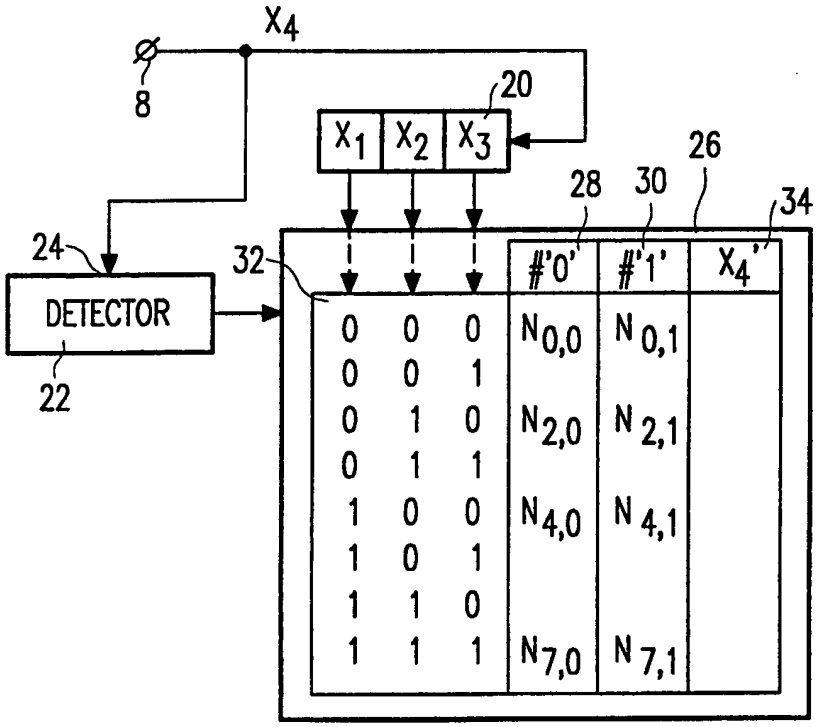

FIG. 2

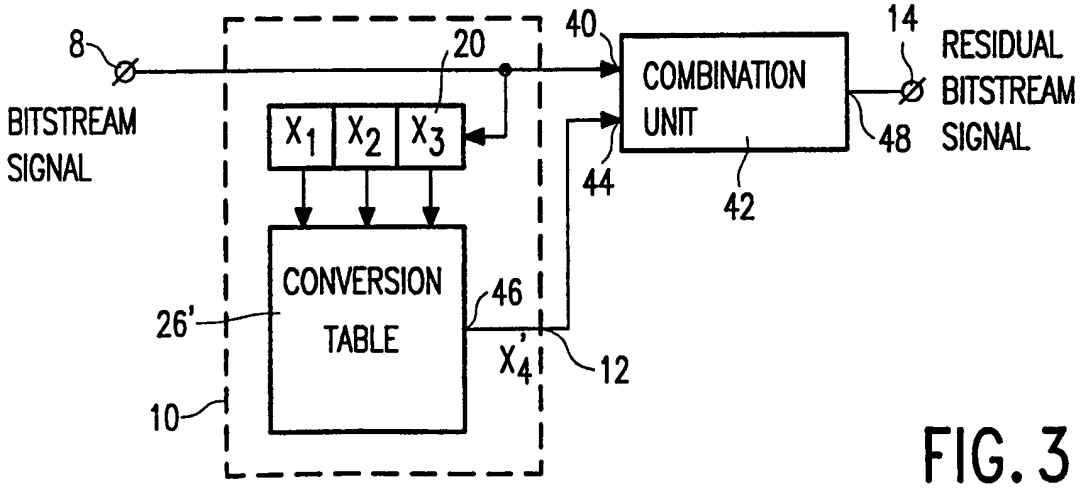

FIG. 3

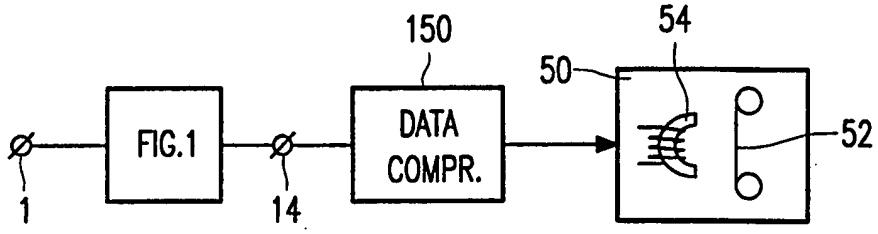

FIG. 4

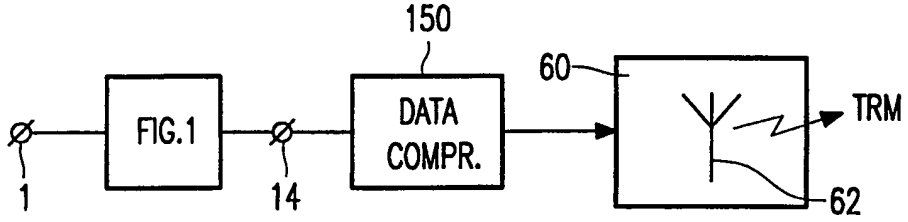

FIG. 5

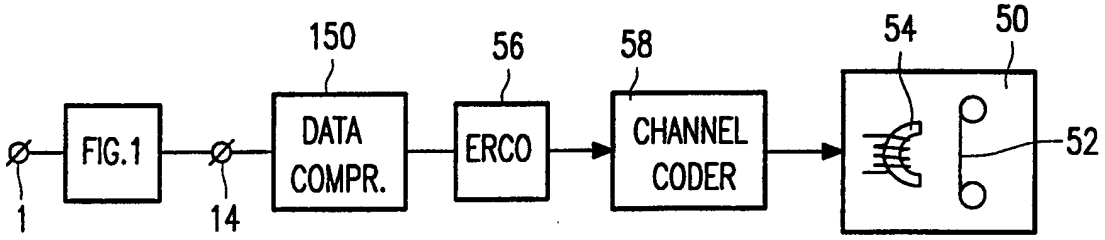

FIG. 6

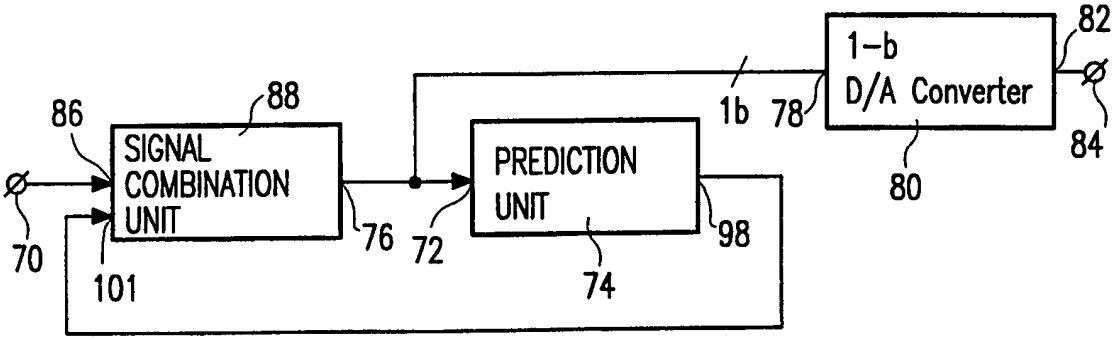

FIG. 7

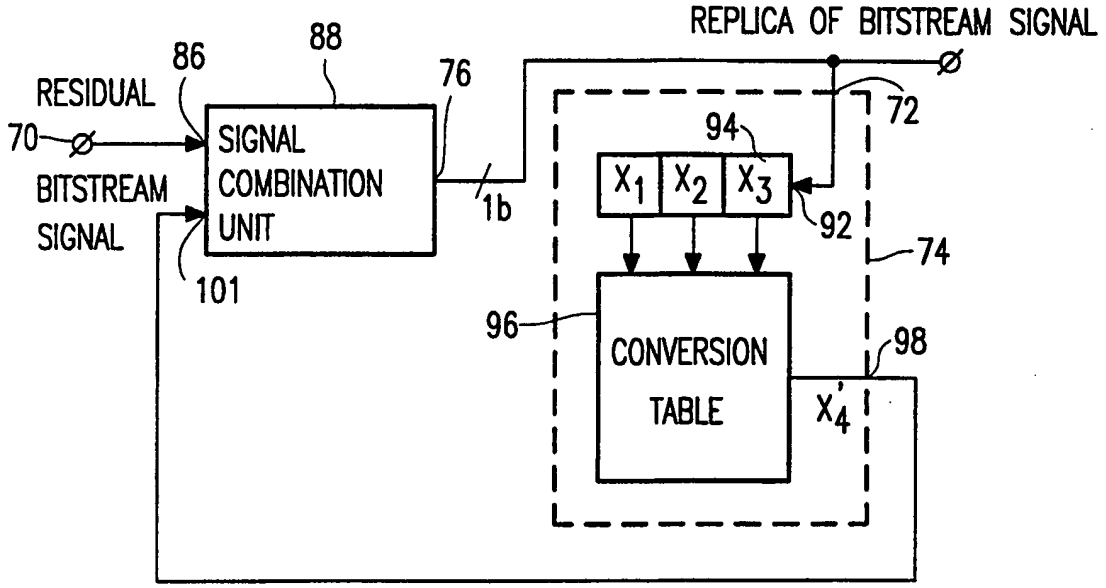

FIG. 8

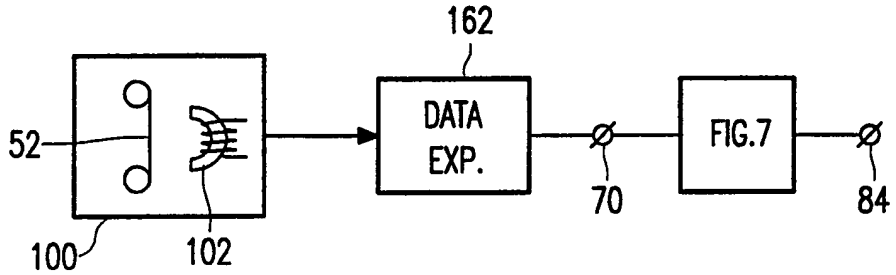

FIG. 9

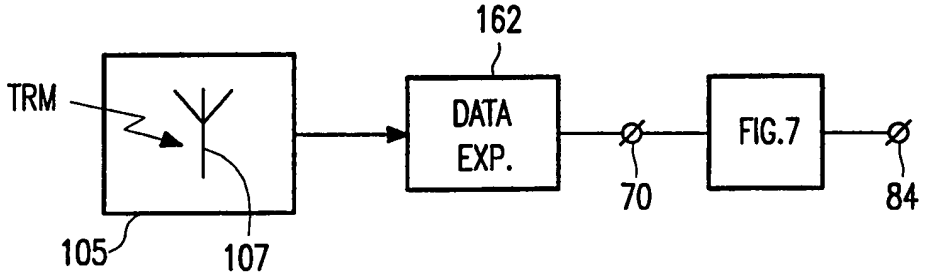

FIG. 10

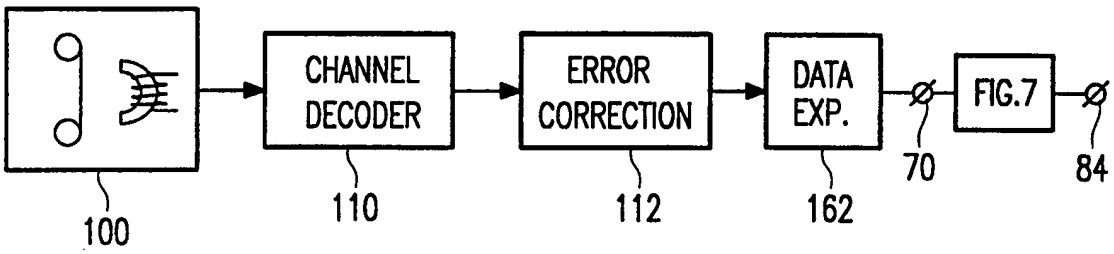
CHANNEL DECODER
ERROR CORRECTION
DATA EXP.
FIG.7
100
110
112
162
70
84

FIG. 11

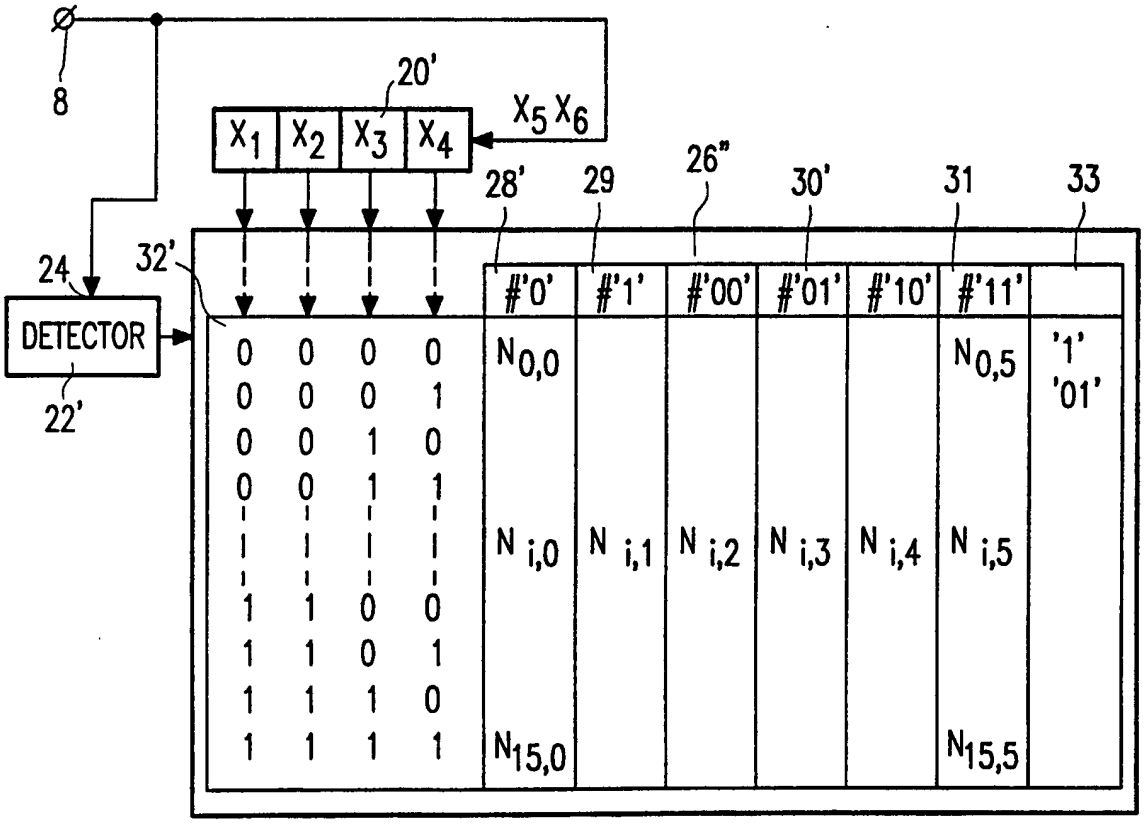
8
20'
X1 X2 X3 X4
X5 X6
28'
29
26"
30'
31
33
24
32'
DETECTOR
22'
#'0'
#'1'
#'00'
#'01'
#'10'
#'11'
0 0 0 0
0 0 0 1
0 0 1 0
0 0 1 1
1 1 0 0
1 1 0 1
1 1 1 0
1 1 1 1
N0,0
N i,0
N15,0
N i,1
N i,2
N i,3
N i,4
N0,5
N i,5
N15,5
'1'
'01'

FIG. 12

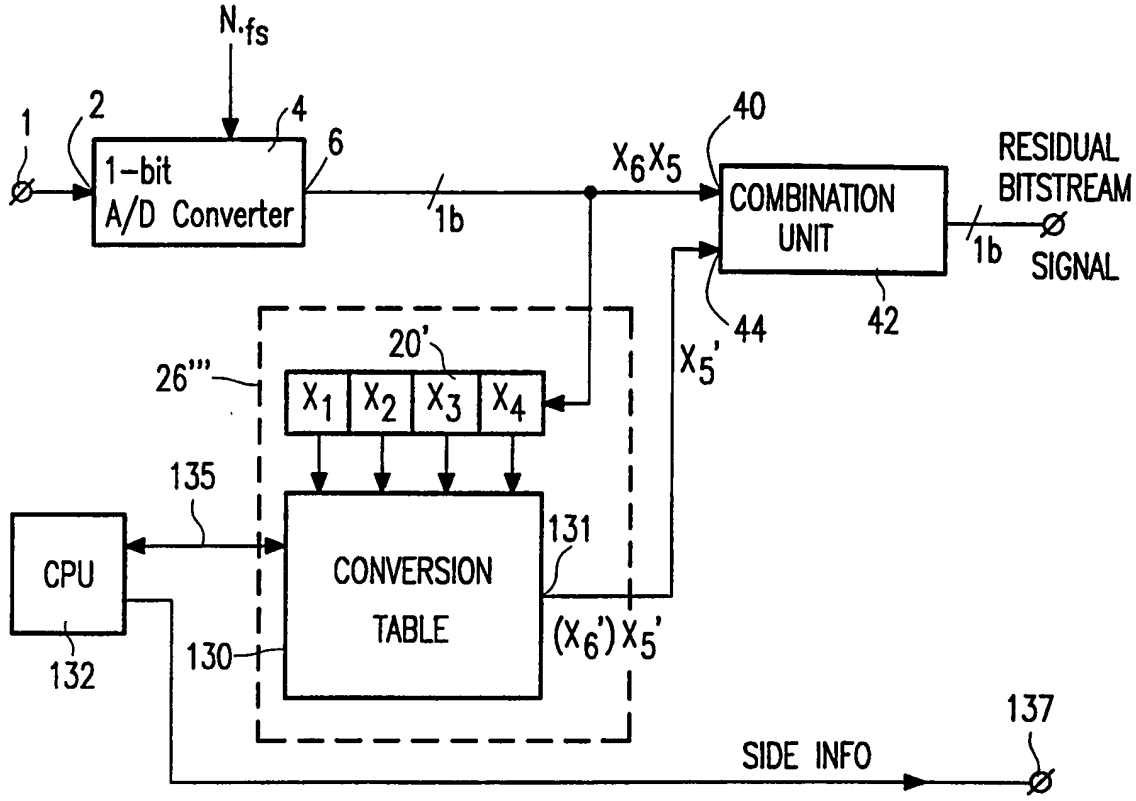
N.fs
1
2
4
6
1-bit
A/D Converter
1b
X6X5
40
COMBINATION
UNIT
RESIDUAL
BITSTREAM
SIGNAL
1b
42
44
X5'
20'
26'''
X1 X2 X3 X4
135
CPU
132
CONVERSION
TABLE
131
130
(X6') X5'
137
SIDE INFO

FIG. 13

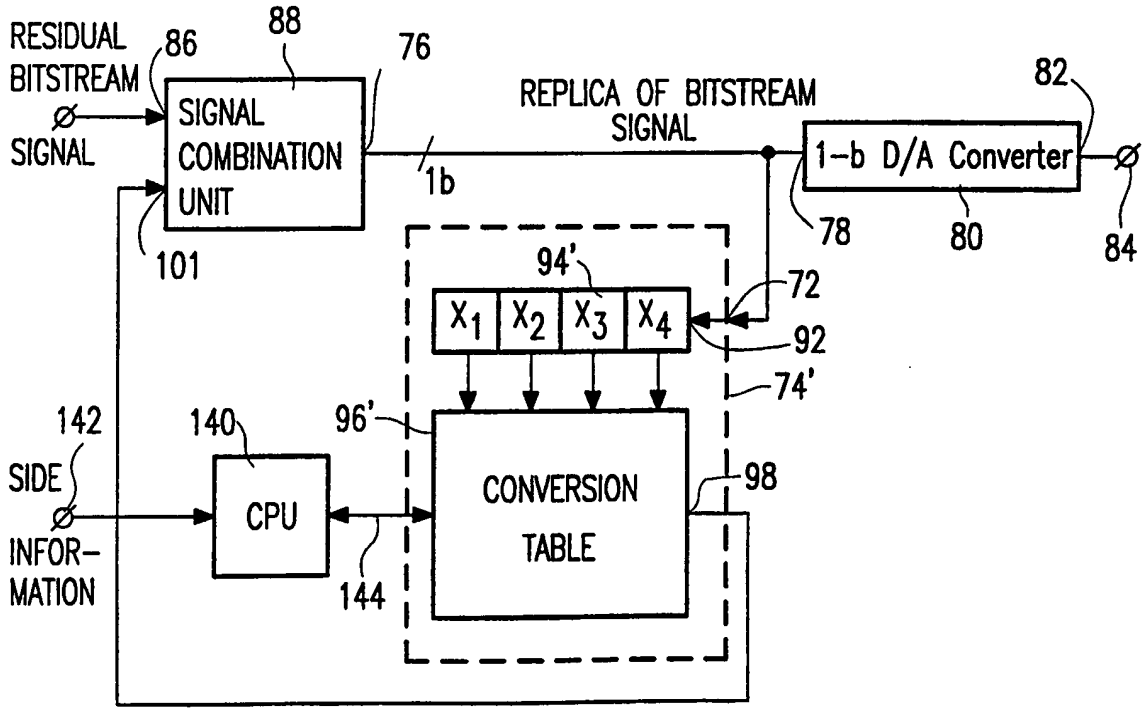
RESIDUAL
BITSTREAM
SIGNAL
86
88
SIGNAL
COMBINATION
UNIT
101
76
1b
REPLICA OF BITSTREAM
SIGNAL
82
1-b D/A Converter
78
80
84
94'
72
X1 X2 X3 X4
92
74'
142
SIDE
INFOR-
MATION
140
CPU
144
96'
CONVERSION
TABLE
98

FIG. 14

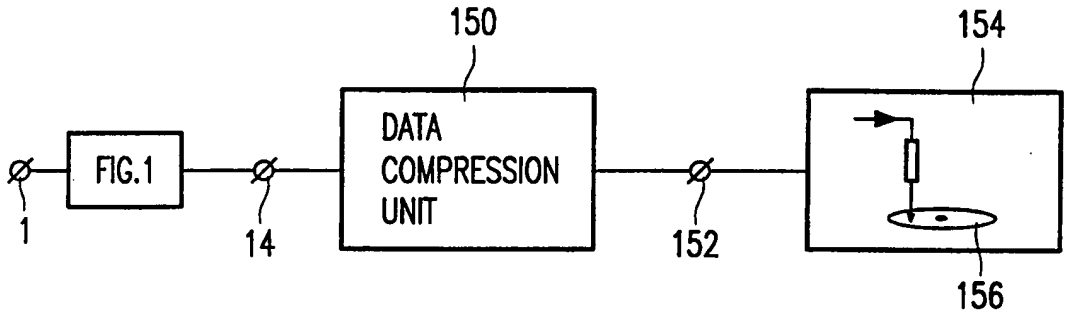
150
154
DATA
COMPRESSION
UNIT
FIG.1
1
14
152
156

FIG. 15

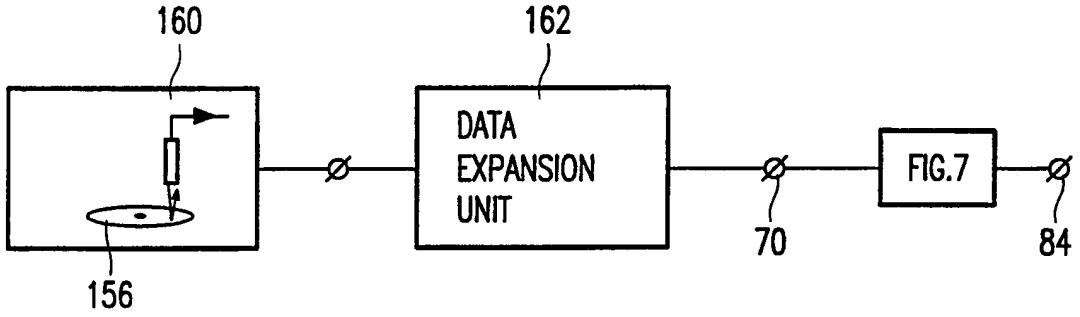
160
162
DATA
EXPANSION
UNIT
FIG.7
156
70
84

FIG. 16

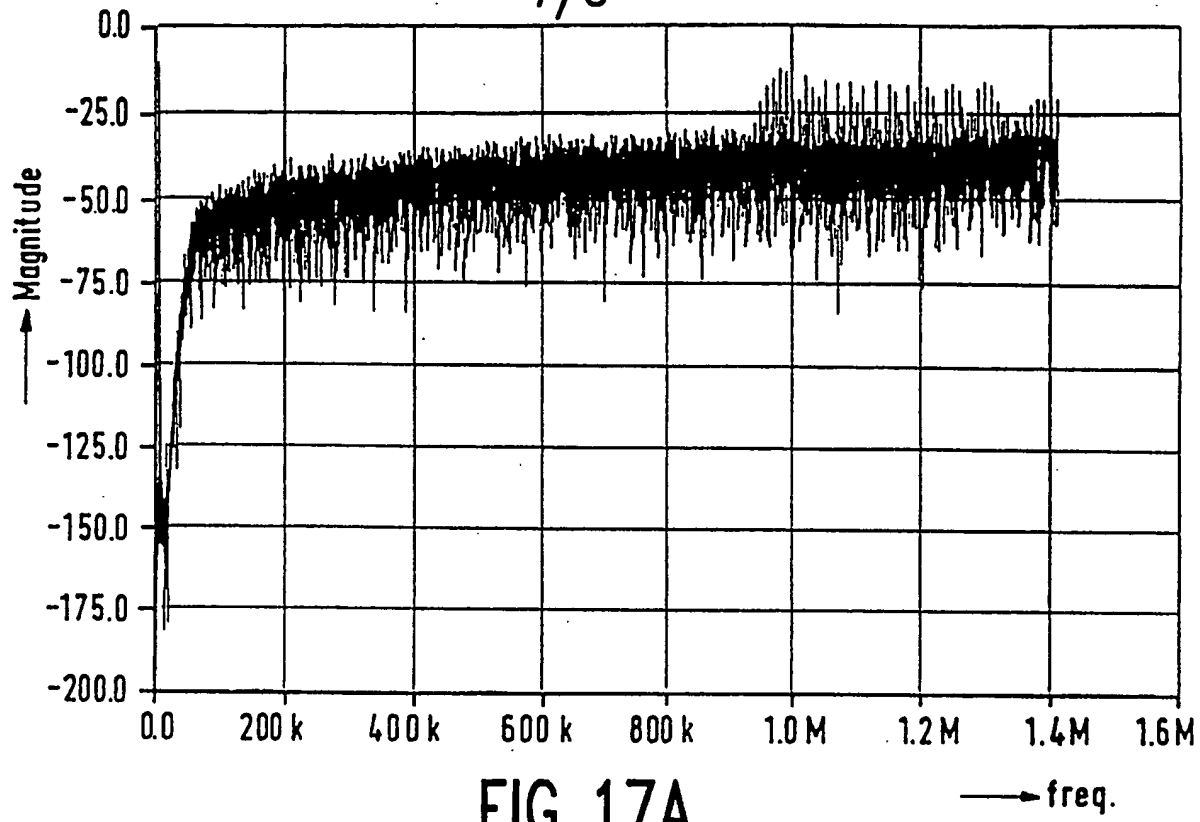

FIG. 17A

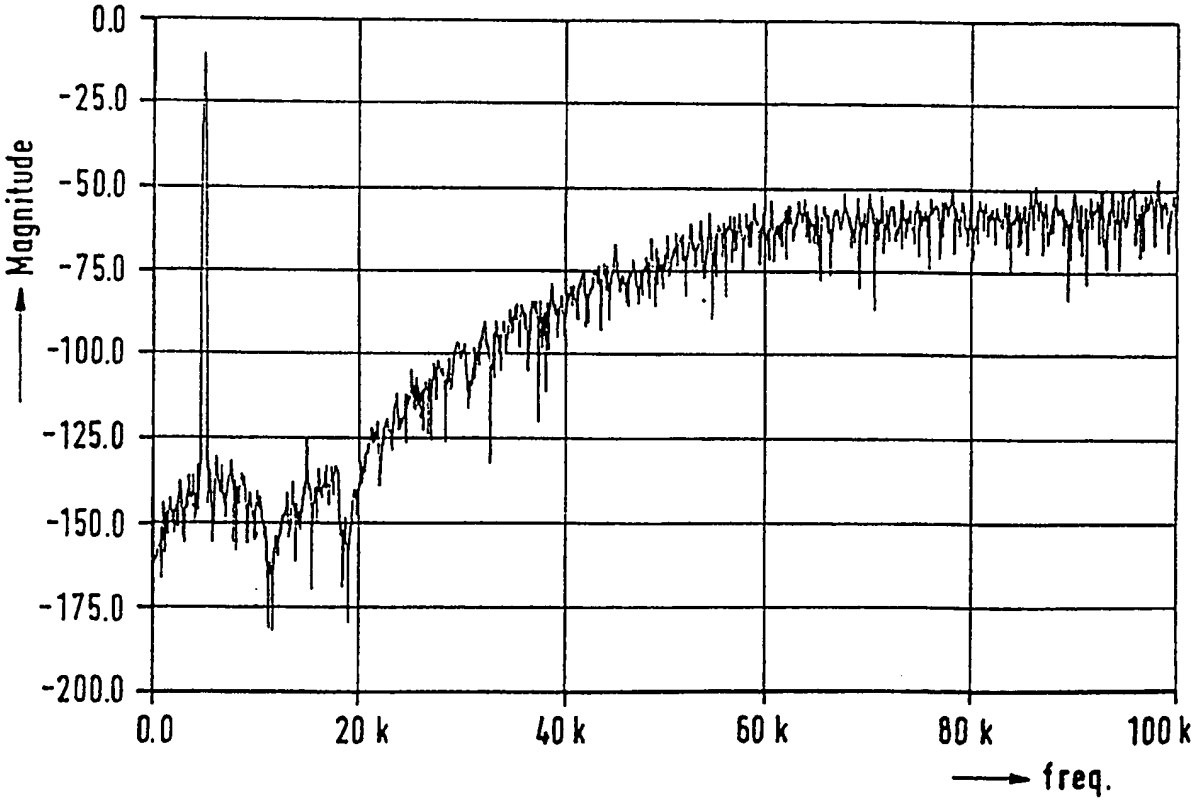

FIG. 17B

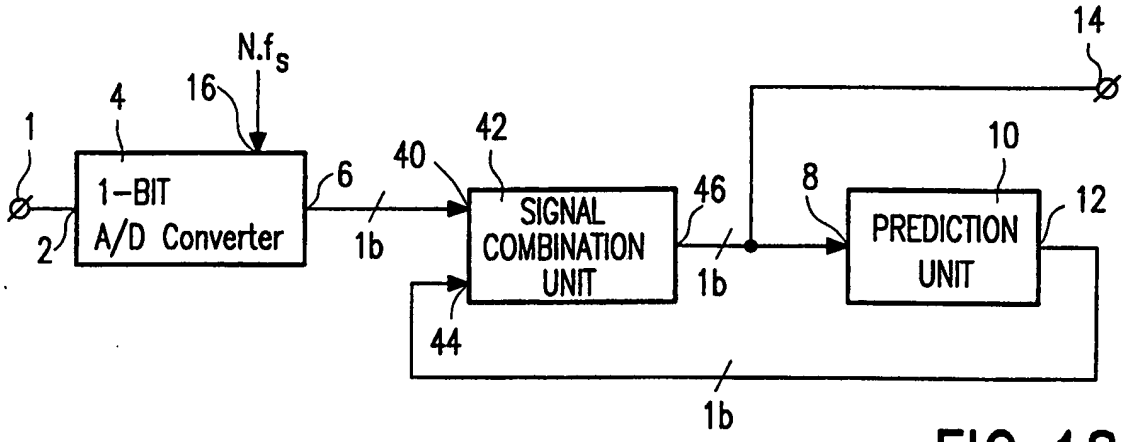

FIG. 18

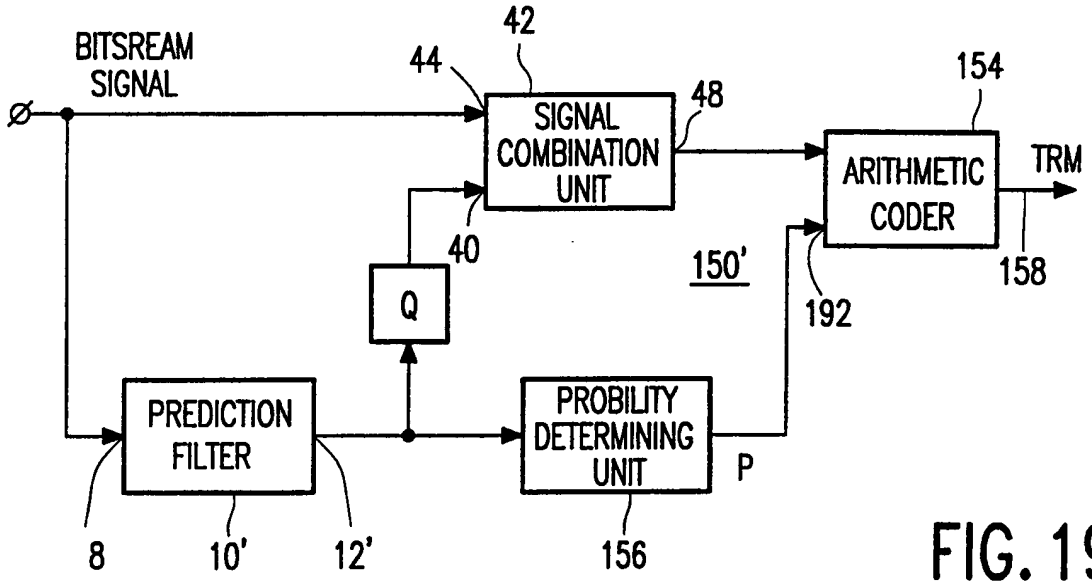

FIG. 19

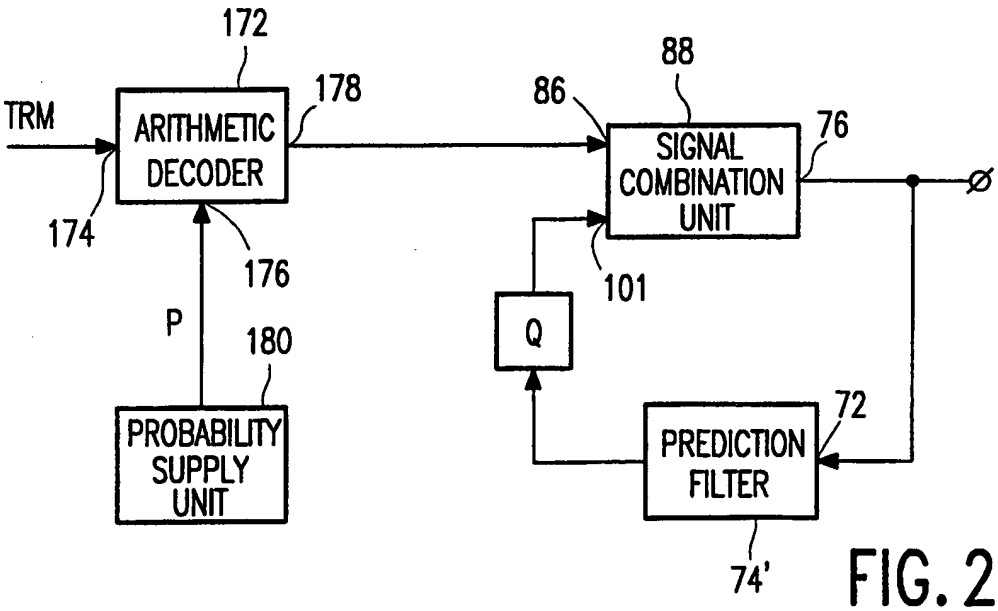

FIG. 20